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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
PIZARRO, RICARDO M

ART UNIT	PAPER NUMBER
2662	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/835,704	MCCLARY ET AL.	
	Examiner	Art Unit	
	Ricardo Pizarro	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/16/01*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-34* is/are allowed.

6)☒ Claim(s) *1-7,9-16,18-21, 35-41 and 43-46* is/are rejected.

7)☒ Claim(s) *8,17,22 and 42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 12 is objected to because of the following informalities: For better reading of the claim, In line 1 delete "the" before [synchronizing]. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by US patent No. 6,539,034 (Shimosaka)

Regarding claim 13, Shimosaka discloses a first and a second unit (units 102-0 and 102-1 in Fig. 1, col 4 line 53) to receive a first and a second signal (Si1 And Si3 in Fig. 1, col 5 line 2), a multiplexing unit coupled to the first and second receiving units (multiplexing unit 103 coupled to units 102-0 and 102-1 in Fig. 1), the multiplexing unit to multiplex the first and second signal (col 5 lines 1-4), a deframing unit coupled to the

multiplexing unit (demultiplexer 105 is coupled to multiplexer 103 in Fig. 1), the deframing unit to deframe the multiplexed first and second signal (col 5 lines 12-15) .

Regarding claim 15, Shimosaka discloses wherein the first and second signals are received at a first rate (signals are received at same clock rate, col 4 line 66)

4. Claim 18 is rejected under 35 U.S.C. 102(e) as being anticipated by US patent No. 4,667,324 (Graves).

Regarding claim 18, Graves a network Multiplex structure comprising generator control circuit to generate a control signal (generator 116 in Fig. 2, col 5 line 18), a first and second receiving unit coupled to the domain clock (Frame stuffer 11 and 13 in Fig. 2, col 5 line 24), the first and second units to receive a first and second signal to synchronize the first and second signal to the clock signal (DS1 and DS1C signals in fig. 2, col 5 line 25); a multiplexer coupled to the first and second receiving unit to the synchronized first and second signals (Multiplexer 10 in Fig. 2 coupled to the first and second receiving units); a deframing unit coupled to the multiplexing means (Demultiplexer 24 in Fig. 2 coupled to multiplexer 10 in Fig. 2).

5. Claims 5 and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by US patent No. 6,667,994 (Farhan)

Regarding claims 5 and 39, Farhan discloses a multiplexing digital communication system comprising; receiving a first and second signal (STS1 510 and DS3 513 in Fig. 5, col 5 lines 4) at a first and second clock rate (STS1 clock rate and DS3 clock rate, col 5 line 7) , multiplexing the first and second signal (at universal

Multiplexer 515 in Fig. 5. col 5 line 14) and deframing the multiplexed first and second signal (at demultiplexer 545 in Fig. 5, col 5 line 22).

6. Claims 2 and 36 are rejected under 35 U.S.C. 102(e as being anticipated by of US patent No. 4,542,500 (Jean-Claude).

The second clock rate (clock 5) is inherently greater that the the clock of input signals ve1-ve4, since it is the clock used to multiplex the input signals to a higher rate multiplex signal

Thus , the claimed limitations of claims 2 and 36 are met by Jean-Claude.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1 , 3 and 4, 35, 36, 37 and 38 are rejected under 35 U.S.C. 103(a) in view of US patent No. 4,542,500 (Jean-Claude).

- Regarding claim 1, Jean Claude discloses receiving a plurality of Signals at a first clock rate (plurality of signals Ve in Fig. 1) synchronizing signals to a second clock rate (signals are synchronized at the rate of clock 5 in Fig. 1) and

deframing the plurality of signals (signal are deframed at demultiplexer as signals Vs in Fig.2).

Jean-Claude does not specifically disclose a machine readable medium, as in claim 1.

However it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the Matsuoka reference by providing to it some kind of readable medium that would have been needed for the system in order to implement t a variety of diverse functions in the system, under computer control, as in claims 1 and 35.

The motivation to do so is obtaining a MUX/DEMUX device that properly operates and follows instructions in order to accomplish the implementation of diverse functions in the system and also enable the reduction of the number of clock lines in the device.

- Regarding claim 35, Jean Claude discloses receiving a plurality of signals at a first clock rate (plurality of signals Ve in Fig. 1) synchronizing signals to a second clock rate (signals are synchronized at the rate of clock 5 in Fig. 1) and deframing the plurality of signals (signal are deframed at demultiplexer as signals Vs in Fig.2).

Jean-Claude does not specifically disclose that the synchronization method described by Jean-Claude is a computer implemented method, as in claim 35.

However since computer implemented tasks are easily manipulated by simply changing program codes, it would have been obvious to one of ordinary skill in the art to

modify Jean-Claude by implementing it through a computer software instead of hardware.

One of ordinary skill in the art would have been motivated to do so because of the flexibility that computer implemented methods offer, they are asily modified without a change in the hardware.

- Regarding claims 4 and 38, Jean-Claude discloses wherein deframing includes cycling through each of the plurality of signals (interpretation of Jean-Claude is that a cycle for deframing purposes s starts when multiplexed data stream data comes in at the input of multiplexer unit in Fig. 2 and completed when all signal exit at the output pf demultiplexer in Fig. 2); deframing each of the plurality of signals in a cycle (all signal are deframed when exiting output of demultiplexer in fig. 2 upon completion of cycle).

- Regarding claim 3 and 37, Jean-Claude discloses a x Mux/Demux system wherein stuffing bits are added to signals(i.e.-justification col 7 lines 21-22).

9. Claims 9 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,667,994 (Farhan).

Regarding claims 9 and 43, Farhan discloses a Multiplexing Digital System comprising: receiving a first signal at a first rate (STS1 signals at STS1 clock rate in Fig. 5, col 5 line 7) , receiving a second signal at a second rate (DS# signal at DS3 clock rate in Fig. 5, col 5 line 7), synchronizing the first and second signal to a third rate

(both signals are synchronized at the clock rat e at 503 in Fig. 5), multiplexing the synchronized first and second signal (multiplexing the signals at Universal multiplexer 515 in Fig. 5, col 5 line 14) and deframing the multiplexed first and second signal (deframing the signals at Demultiplexer 545 in Fig. 5, col 5 lines 20-21).

Farhan does not specifically disclose a machine readable medium as in claims 9 and 43.

Therefore it would have been to a person of ordinary skill in the art at the time of the invention modify the Farhan reference by providing certain kind of computer readable medium in order to implement a variety of instructions for the system to be properly operated under computer control..

10. Claims 7, 10-11 and 41, 44-45 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,667,994 (Farhan).

Farhan does not specifically disclose the third clock rate being greater than the first and second clock rate, as in claims 7 ,11 and 45 ; first and second rate are approximately equal, the sum being less that the third rate, as in claims 10 and 41. 44,

However , it would have been obvious to one of ordinary skill in the art that the clock rates could have been adjusted according to the needs of the system to prevent an underflow situation

The motivation to do so is obtaining a MUX/DEMUX device that performs and provides adequate synchronization in the system .

11. Claims 6 and 40 are rejected under 35 U.S.C. 103(a) as being

unpatentable over US patent No. 6,667,994 (Farhan). in view US patent No. 6,539,034 (Shimosaka)

Farhan does not disclose the first and second clock rate being the same clock rate, as in claim 6 and 40.

However Shimosaka discloses the reception of signals at the same clock rate (col 4 line 65), as in claims 6 and 40

Therefore, it would have been obvious to one of ordinary skill in the art to modify the Farhan reference by providing the same clock rate as in Shimosaka in order to enable a large reduction in the number of clock lines in the Mux/Demux device.

The motivation to do so obtain proper synchronization in the system.

12. Claims 8 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6, 667,994 (Farhan). in view of US patent No. 4,542,500 (Jean-Claude).

Farhan does not specifically disclose synchronizing the first and second signals to a third clock rate before multiplexing the first and second signals,

However Jean-Claude discloses a multiplexing and demultiplexing circuit, comprising a first and a second signal that are synchronized to a third clock rate before multiplexing((Signal Ve2 and Ve3 at clock rate Fe2 and Fe3 respectively are synchronized to the clock rate of clock 5 before multiplexing at multiplexer 7 in fig. 1, col 3 lines 35-38 and 58-60)

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to modify the Farhan reference by synchronizing both signals to a third clock rate to have the system to multiplex and demultiplex signals between low rate digital synchronous signals and high rate plesiochronous digital signals.

The motivation to so is to justify or correct the signals timing during multiplexing operations in the device.

13. Claims 12 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,667,994 (Farhan) in view of US patent No. 4,542,500 (Jean-Claude).

Farhan did not disclose the synchronizing including adding stuffing bits to the signals, as in claims 12 and 46.

However, Jean-Claude discloses a Mux/Demux system wherein stuffing bits are added to signals, as in claims 12 and 46 (col 7 lines 21-22)

Therefore, it would have been obvious to one of ordinary skill in the art to modify the Farhan reference by providing stuffing bits to signals as discloses by Jean-Claude to have the system using a single stage MUX/DEMUX , for both synchronous and asynchronous bit streams.

The motivation to do so is to obtain a multiplexed structure for multiplexing bit stream from a plurality of tributaries into a multiplexed bit stream

14. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,539,034 (Shimosaka) in view US patent No. 6,667,994 (Farhan).

Shimosaka does not specifically disclose the first and second signal being received at a first and second rate.

However Farhan discloses a first and a second signal (STS1 and DS3 in Fig. 1) being received at a first and at a second clock rate (col 5 lines 7)

Therefore it would have been obvious to a person of ordinary skill in the art to mofidy the Shimosaka reference by providing a first signal at a first clock rate and a second signal at a second clock rate as in Farhan , to be able have a MUX/DEMUX device to be used in the transmission of multiple digital and/or analog input signal on a single high speed or optical channel.

The motivation to do so is to obtain a circuit that can be incorporated in a particular system and that can be applied to other systems having different input clock rates.

15. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6,539,034 (Shimosaka) in view of US patent No. 6, 034,974 (Matsuoka).

Shimosaka does not specifically disclose a domain clock to transmit a clock signal , a first and second receiving unit coupled to the domain clock , the first and second units to receive a first and second signal to synchronize the first and second signal to the clock signal, neither the domain clock being faster that a sum of the first rate of the first signal and a second rate of the second signal, as in claim 16

However, Matsuoka discloses a Channel selection type demultiplexing circuit, comprising a domain clock to transmit a clock signal (Clock signal clk-in in putted to

the Control Circuit in Fig. 1, col 6 line 32), a first and second receiving unit coupled to the domain clock (DMUX-1 Bit demultiplexing circuit and DMUX-N Bit Demultiplexing circuit in Fig. 1, col 7 line 11) , the first and second units to receive a first and second signal to synchronize the first and second signal to the clock signal (Clock signal C1 and Cn synchronized to clock signal clk-in in Fig. 1).

Therefore it would have been obvious to one of ordinary skill in the art to modify the Matsuoka reference by providing a domain clock with the characteristics disclosed in Matsuoka in order to have the demultiplexing circuit of Shimosaka able to process a higher number of streams.

The motivation to do so is to obtain a demultiplexing circuit capable of obtaining appropriate synchronization.

16. Claims 19 and 21 are is rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6, 034,974 (Matsuoka).

Regarding claim 19, Matsuoka discloses wherein the first and second signals are received at a second and third clock rate (Clock rates C1 and Cn in Fig. 1).

Matsuoka does not specifically disclose, the sum of the second and third clock rate being less than a rate of the clock signal, as in claim 19; wherein the clock signals's rate is greater that a sum of the first and second signals's rate, as in claim 21.

However ,it would have been obvious to one of ordinary skill in the art that the having the clock signal being higher than the sum of the first and second clock rates would have allowed an underflow situation in the system.

The motivation to do so is obtaining a MUX/DEMUX device that provides reduction of the number of clock lines in the device.

17. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over US patent No. 6, 034,974 (Matsuoka). in view of US patent No. 4,542,500 (Jean-Claude).

Matsuoka does not disclose the synchronizing including adding stuffing bits to the signals, as in claim 20.

However, Jean-Claude discloses a x Mux/Demux system wherein stuffing bits are added to signals(i.e.-justification col 7 lines 21-22), as in claim 20.

Therefore, it would have been obvious to one of ordinary skill in the art to modify the Matsuoka reference by providing stuffing bits to signals as discloses by Jean-Claude to have the system using a single stage MUX/DEMUX , for both synchronous and asynchronous bit streams.

The motivation to do so is to obtain a multiplexed structure for multiplexing bit streams from a plurality of tributaries into a multiplexed bit stream

Allowable Subject Matter

18. Claims 23-34 are allowed.

19. Claims 8, 17, 22, 42 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US patent No. 4,667,324 discloses a Network multiplex structure.
- US patent No. 5,001,711 discloses a complex Multiplexer/Demultiplexer apparatus.
- US patent no. 6,275,510 discloses a telecommunications multiplexer.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(571) 273-8300

(for formal communications intended for entry, for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to 220 South 20th Street, Crystal Plaza Two, Lobby, Room 1B03, Arlington, Va 22202 (Customer Window).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Ricardo Pizarro** whose telephone number is (571) 272-3077. The examiner can normally be reached on Monday-Friday from 9:00 AM to 5:30 PM. .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Hassan Kizou** can be reached on (571) 272-3088

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 6, 2005
Ricardo Pizarro

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